WHAT IS CLAIMED IS:

1. An interconnect structure comprising

a buried etch stop layer comprised of a polymeric material having a composition $Si_vN_wC_xO_yH_z$, where $0.05 \leq v \leq 0.8$, $0 \leq w \leq 0.9$, $0.05 \leq x \leq 0.8$, $0 \leq y \leq 0.3$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$;

a via level interlayer dielectric that is directly below said buried etch stop layer;

a line level interlayer dielectric that is directly above said buried etch stop layer; and

conducting metal features that traverse through said via level interlayer dielectric, said line level interlayer dielectric, and said buried etch stop layer.

2. The interconnect structure of claim 1 wherein said polymeric material is selected from a group consisting of: polysilazanes, polysilanes, polycarbosilanes, polysilasilazane, polysilylenemethylenes, polysilacarbosilanes, polysilylcarbodiimides, polysiloxazanes, polycarbosilazanes, polysilylenemethylenes, polysilsesquiazane, and polysilacarbosilazanes.

3. The interconnect structure of claim 1 wherein said buried etch stop layer comprises one of: polyureamethylvinylsilazane (KiON), polyallylhydridocarbosilane or polycarbomethylsilane.

4. The interconnect structure of claim 1 wherein said buried etch stop layer has a dielectric constant ranging from about 1.4 and about 2.2.

5. The interconnect structure of claim 1 wherein said buried etch stop layer has a dielectric constant ranging from about 2.2 to about 3.8.

6. The interconnect structure of claim 1 wherein said buried etch stop layer is porous.

7. The interconnect structure of claim 1 wherein adhesion promoters are positioned on an interface of said buried etch stop layer.

8. The interconnect structure of claim 1 wherein said buried etch stop layer and said via level interlayer dielectric have an identical pattern.

9. The interconnect structure of claim 1 wherein said buried etch stop layer is permeable to low molecular weight volatile products.

10. The interconnect structure of claim 1 wherein said buried etch stop layer is thermally stable to temperatures greater than about 350°C.

11. The interconnect structure of claim 1 wherein said via level interlayer dielectric and said line level interlayer dielectric are identical materials.

12. The interconnect structure of claim 1 wherein said via level interlayer dielectric and said line level interlayer dielectric are different materials.

13. The interconnect structure of claim 1 wherein said buried etch stop layer has a thickness of about 5.0 nanometers to about 50.0 nanometers.

14. The interconnect structure of claim 1 wherein said via level interlayer dielectric, said line level interlayer dielectric or a combination of said via level interlayer dielectric and said line level interlayer dielectric each have a thickness ranging from about 30 nanometers to about 500 nanometers.

15. The interconnect structure of claim 1 wherein said conducting metal features are selected from the group consisting of: copper, aluminum, gold, silver, and alloys thereof.

16. The interconnect structure of claim15 wherein said conducting metal features have a lining comprising a metal containing barrier layer, wherein said metal containing barrier layer is selected from a group consisting of: tantaulum, tungsten, ruthenium, cobalt, and titanium.

17. A method for generating an interconnect structure comprising:

depositing a via level interlayer dielectric;

depositing a buried etch stop layer atop said via level interlayer dielectric by a solvent based approach, said buried etch stop layer comprising a polymeric material having a composition $Si_vN_wC_xO_yH_z$, where $0.05 \leq v \leq 0.8$, $0 \leq w \leq 0.9$, $0.05 \leq x \leq 0.8$, $0 \leq y \leq 0.3$, $0.05 \leq z \leq 0.8$ for $v+w+x+y+z=1$;
depositing a line level interlayer dielectric atop said buried etch stop layer.

18. The method of claim 17 wherein said deposition of said via level interlayer dielectric, said line level interlayer dielectric, or a combination of said line level interlayer dielectric and said via level interlayer dielectric is by a solvent based approach.

19. The method of claim 17 wherein the said solvent based approach comprises a solution having an organic solvent selected from a group consisting of: propylene glycol methyl ether acetate (PGMEA), propylene glycol methyl ether (PGME), toluene, xylenes, anisole, mesitylene, butyrolactone, cyclohexanone, hexanones, ethyl lactate, and heptanones.

20. The method of claim 17 wherein said solvent based approach comprises spin coating, spray coating, scan coating, or dip coating.

21. The method of claim 19 further comprising annealing said via level interlayer dielectric, said line level interlayer dielectric, said buried etch stop layer, or a combination of said line level interlayer dielectric, said via level interlayer dielectric and said buried etch stop layer by a process selected from the group consisting of: thermal curing, electron irradiation, ion irradiation, or irradiation with ultraviolet or visible light.

22. The method of claim 21 wherein at least one of said via level interlayer dielectric, said buried etch stop layer, or said line level interlayer dielectric crosslink during said annealing.

23. The method of claim 17 wherein an adhesion promoter is used to enhance adhesion of said buried etch stop layer to said via level interlayer dielectric or line level interlayer dielectric, wherein said adhesion promoter comprises $Si_xL_yR_z$, wherein L is selected from the group consisting of hydroxy, methoxy, ethoxy,

acetoxy, alkoxy, carboxy, amines and halogens, and R is selected from the group consisting of hydrido, methyl, ethyl, vinyl, and phenyl (any alkyl or aryl).

24. The method of claim 17 wherein said solvent based approach further comprises an antistriation agent.

25. The method of claim 17 wherein a dual damascene integration approach is utilized to generate said interconnect structure, wherein patterns are defined in at least one hardmask layer and subsequently transferred by dry etch processes into said line level interlayer dielectric, said buried etch stop layer, and said via level interlayer dielectric.

26. The method of claim 25, wherein said dual damascene integration is performed with a full via level interlayer dielectric etch followed by a line level interlayer dielectric etch.

27. The method of claim 25, wherein the said dual damascene integration involves dry etch processes involving a reactive plasma that are used to define the line level interlayer dielectric, buried etch stop layer, and via level interlayer dielectric.

28. The method of claim 17, wherein said buried etch stop layer etches at least about five times slower than said line level interlayer dielectric.

29. The method of claim 17, wherein said buried etch stop layer etches at least about five times slower than said via level interlayer dielectric.

30. The method of claim 17, wherein said buried etch stop layer etches at least about five times slower than a cap barrier layer.